Circuit Emulation Services Module

TEJAS® NETWORKS

Future Ready. Today

Introduction

As mobile backhaul transitions to a packetized infrastructure, it becomes important to efficiently carry TDM signals on a packet switched network. This will require an ability to convert TDM to packet formats while maintaining accurate synchronization information for these circuits. Also, TDM requires low latency and jitter for reliable transmission and this can only be achieved by guaranteeing adequate bandwidth, prioritization and buffering along the end-to-end path to minimize packet losses, delays or reordering. TDM emulation in LTE would also impose additional expectations typical of circuit services such as performance monitoring as per ITU G.775, service restoration times within 50ms, service quality considerations based on jitter, wander and BER as per ITU G.703, support for service loopbacks at the TDM interface etc.

While packet-based multimedia services would form a large proportion of traffic carried on a 3G/4G network, there would continue to be a definite requirement to transport legacy voice and TDM services from co-located 2G base stations for several years to come. In such cases, the Tejas equipment shall provide a means to subsume these services over the packet switched network using Circuit Emulation or TDM over Packet mapping.

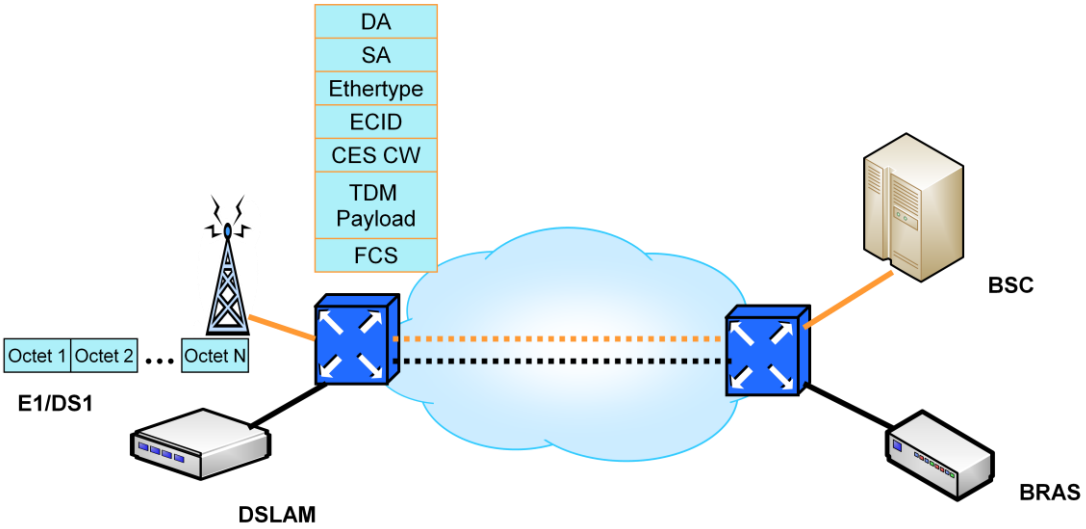
Circuit Emulation Approaches:

a. **SAToP (IETF RFC4553):** SAToP stands for Structure Agnostic TDM over Packet. SAToP is an encapsulation method used for transparently carrying a TDM signal without processing the DS0 timeslots within. SAToP packetizes the incoming TDM stream, such as an E1, in chunks of say 256 bytes and creates a packet stream with a suitable header. A special Emulation Identifier field is used to indicate the presence of a TDM channel along with a control word to detect losses or misordering of packets at the far end. A SAToP link is relatively easy to provision. The performance of a SAToP implementation is a function of the jitter buffer size and packetization length parameters that have a direct impact on signal latency and delay variations. In general, both

packetization length parameters that have a direct impact on signal latency and delay variations. In general, both these parameters have to be configurable to allow the performance to match service quality requirements.

CESoPSN (IETF RFC5086): CESoPSN is an alternate encapsulation technique that relies on an "awareness" of the underlying TDM signal structure to permit a more bandwidth efficient transmission of select timeslots e.g., DS0s within an E1. The CESoPSN approach helps strip off the TDM overhead and extract the voice payloads thus resulting in a better use of transport bandwidth, fewer circuits, and superior network aggregation. This is especially important in networks where there are bandwidth constraints such as mobile access. But at the same time CESoPSN also requires the IWF function to participate in the handling of signaling, timing and fault detection (alarm) functions. CESoPSN implements a TDM framing function to discover the frame alignment signal and the individual timeslots and thus ensures alignment of the packetized CES stream with the TDM structure so detected. At the other end, the device with CESoPSN uses a local frame generator to recreate the TDM frame structure and fills it with DS0s from the packet stream. Accurate clock recovery is required to prevent bit errors and excessive jitter and wander.

CESoETH (MEF 3 and MEF 8): CESoETH defines the mechanism for carrying TDM traffic over native Ethernet networks using an ECID parameter that identifies the CES service being transported. While MEF 3 describes the CES requirements, implementation level details are specified in MEF 8 with respect to connectivity, timing, synchronization, performance criteria and service OAM. CESoETH is built on the same principles as SAToP and CESoPSN. Both structure-agnostic and structure-aware modes of operation are defined. CESoETH is interoperable with SAToP and CESoPSN. MEF 3 and MEF 8 ensure integrity of TDM data with the ability to access performance monitoring payloads available within the TDM layer for PDH & SDH/SONET services. TDM interfaces supported range from E1/DS1 to STM-4/OC-12.



Circuit Emulation Functions:

The Circuit Emulation Interworking Function (CES IWF) is defined as the adaptation function that interfaces the CES application to the PSN. The CES IWF is responsible for all the functions required for the emulated service to operate.

Payload Formation and Extraction: The IWF packetizes the TDM stream by buffering data needed to form a CES packet. As a part of extraction, it maintains a jitter buffer to compensate the packet delay variations introduced in the MEN. Using the sequence number in the received frames, lost frames and out of order frames are detected. A pre-configured pattern is inserted in the place of lost frames to maintain the data integrity and the output TDM rate. Re-ordering is done for the out-of-order frames. Synchronization of the TDM Streams: Synchronization is an important consideration in any circuit emulation scheme. Put simply, the clock used to play out the data at the TDM interface must be the same frequency as the clock used to input the data at the TDM interface at the source IWF, otherwise frame slips will occur over time.There are four basic options for the transmit clock on TDM interface: Clock Recovery: There are two methods of clock recovery available while recovering the timing from the CES packets:

Adaptive Clock Recovery: In this method, the TDM service clock is recovered based on the jitter buffer fill level. Since the MEN introduce delay variations, the jitter buffer fill levels keep varying continuously. The TDM service clock is recovered after filtering the variations. The accuracy of the recovered clock depends on the delay-variations that are introduced by the MEN. Hence the Adaptive clock recovery method is dependent on the QoS treatment given to the CES frames in the MEN. In Tejas CPO, the CES traffic is mapped to low latency queues that introduce minimal delay-variations and packet loss.

Differential Clock Recovery: In this method, a known clock source (reference clock) is available at the two terminating IWFs. Rate difference between the service clock and the reference clock is encoded in the optional RTP header. During extraction, this information is used to determine the TDM service clock. Differential mode of clock recovery is not dependent on the delay variation introduced by the MEN, so the recovered clock is more accurate than that recovered with the adaptive clock. The reference clock can be provided using various synchronization sources like SyncE clock, 1588v2, BITS interface using local PRC.

A full CES implementation from Tejas:

Tejas supports both structure-agnostic and structure-aware emulation services as per relevant standards discussed above. Hence, the implementations are fully interoperable with third-party standards-based offerings. Emulation of E1s circuits is possible. Adaptive Clock Recovery (ACR) or Differential Clock recovery (DCR) is used for clock extraction. The CES module has a stable clock source with temperature controlled crystal oscillators. Tejas implementation of CESoPSN supports PCM30 and PCM31 framing of E1s with flexible and fully reconfigurable timeslots and the ability to raise alarms for E1s. Synchronization information of these packetized TDM signals is maintained and

distributed end-to-end through packet-based methods or Synchronous Ethernet (SyncE) as defined in physical layer standards ITU G.8261 and ITU G.8262.

Tejas supports the Circuit Emulation Services (CES) module in its Carrier Ethernet (TJ2000) and POTP (TJ1400) series of platforms. The key technical specifications are shown below.

Feature	SAToP	CESoPSN
Physical Interfaces	E1, STM-N	E1, STM-N
Jitter Buffer	Configurable upto 128ms	Configurable upto 128ms
Clock recovery	Configurable ACR/DCR	Configurable ACR/DCR
Packetization Length	Configurable	Configurable
Framing Modes	N.A	PCM30, PCM31
Synchronization	SyncE, 1588v2	SyncE, 1588v2
Standards	IETF RFC4553	IETF RFC5086